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Design and Performance Analysis of Inexact-Speculative Han Carlson Adder

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ABSTRACT

Low power and high speed design is one of the important building blocks in digital circuits. In conventional Inexact speculative adder based on Carry look-ahead adder to consume more power issues and longest critical path delay. In this paper, Han Carlson adder based design of the proposed ISA architecture which is fine grain pipelined because to increase the processing speed and reduces the complexity, silicon area and power consumption. Additionally this architecture has been clock gated giving rise to dynamic power reduction opportunity. Functional verification and synthesis of suggested ISA is carried out on 45nm CMOS technology by using Tanner EDA tool.

Keywords-Inexact speculative adder(ISA), Han Carlson adder(HCA), Pipelining, clock gated.

I.INTRODUCTION

In electronics, an adder is a digital circuit that performs addition of binary numbers. In many computers and other kinds of processors [1], adders are used not only in the arithmetic logic units, but also in other parts of the processors, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. High speed adders are highly desirable in the present day scenario, though power and silicon area are equally vital. Spectrum sensors used in intelligent cognitive-radio environment as well as internet of everything (IOE) devices focused on physical interfaces are largely-explored research areas in the recent time [2]. With tolerable degradation in accuracy and performance, it is feasible to conceive high-speed, low power and area efficient design using inexact and approximate circuit technique [3]. Accuracy of such circuits can be traded off to improve the power and speedby speculation. Thereby, such adders are referred as inexact speculative adder (ISA). However, there is space to further improve the speed of such adders by retaining the accuracy with minimum error. Thereafter, this inexact speculative adder is fine grain pipelined to reduce the critical path delay that further enhances the operating speed. Subsequently, clock signal fed to various stages of the deep pipelined ISA-architecture has been gated to reduce the power consumption [4]. Speculative adders exploit the fact that the typical carry propagation chain of an addition does not span the whole length of the adder, making it is possible to estimate an intermediate carry using a limited number of previous stages. Thus, the carry propagation chain, which is the critical path of the adder [5], can be split into two or more shorter paths, relaxing constraints over the entire design, reducing glitching power, and improving the Energy-Delay-Area-Product (EDAP) beyond the exact adders.

II.PREVIOUS WORK

In this design, CLA which is fine grain pipelined to include few logic gates along its critical path and thereby enhancing the frequency of operation. By calculating carry signals advance based upon input bits and does not wait for the input signals to propagate through different stages. Fine grain pipelining can be to increase the processing speed. Also, a CLA is a fast parallel adder as it reduces the propagation delay by more complex hardware, hence it is costlier as shown in figure5. Parallel adder is the binary addition of two numbers is initiated when all the bits of the augend and the addend must be available at the same time to perform the computation. To avoid the ripple carry is carry-look ahead which computes some of the carry values

directly from the inputs without waiting on the previous carries.

If a sequence of bits is all 1's, there will be a carry from the sequence, when it is incremented. Conversely, if there is a 0 anywhere in the sequence, any intermediate carry will be "extinguished". By

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III. DESIGN APPROACH OF THE PROPOSED ISA

improves hardware efficiency upon the state-of-the-art and introduces a new way to control errors. Taking advantage of such circuits would help to realize extremely energy-efficient and high performance DSPs and hardware accelerators at lower integration cost and with higher speed, data rate or duty-cycling.

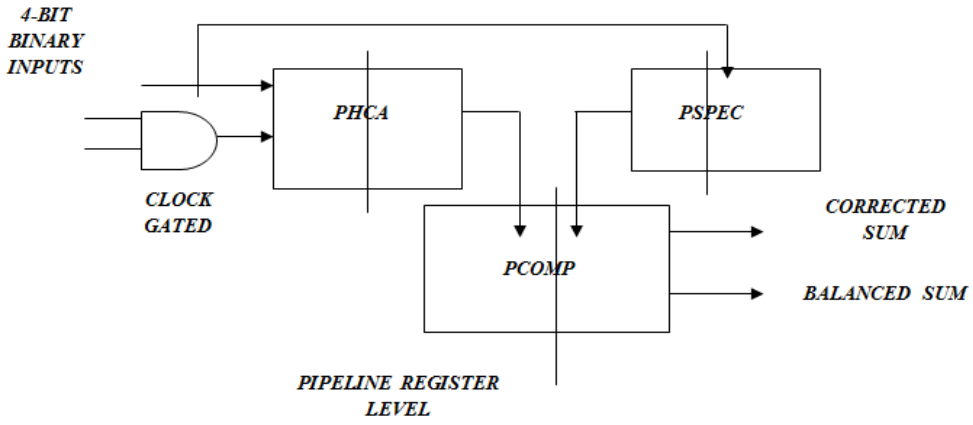

Figure 1: VLSI Architecture for Inexact Speculative Han Carlson Adder

A.PIPELINED HAN CARLSON ADDER

Han Carlson adder combines the brent kung and kogge stone structure into hybrid structure. It is efficient and suitable for VLSI implementation and consist of three stages pre-processing, prefix-processing and post-processing. The Pre-Processing and Post-Processing Stages of a Prefix adder involve only simple operations on signals to each bit location. Hence, adder performs mainly on Prefix operation as shown in figure2. It reduces the number of prefix operation by using more number of brent-kung adder stages and lesser number of kogge stone stages. This adder is different from Kogge-Stone adder in the sense that these performs carry-merge operations on even bits and generate/propagate operation on odd bits. At the end, these odd bits recombine with even bits carry signals to produce the true carry bits.

It also reduces the complexity,silicon area and power consumption significantly. Kogge stone and brent kung adder reduces the area required by the adder circuitry. Han-Carlson adder constitutes a good trade-off between fan out, number of logic levels. Because of this, Han-Carlson adder can Achieve equal speed performance respect to Kogge-Stone adder, at lower power consumption and area. Therefore it is interesting to implement a speculative Han-Carlson adder.

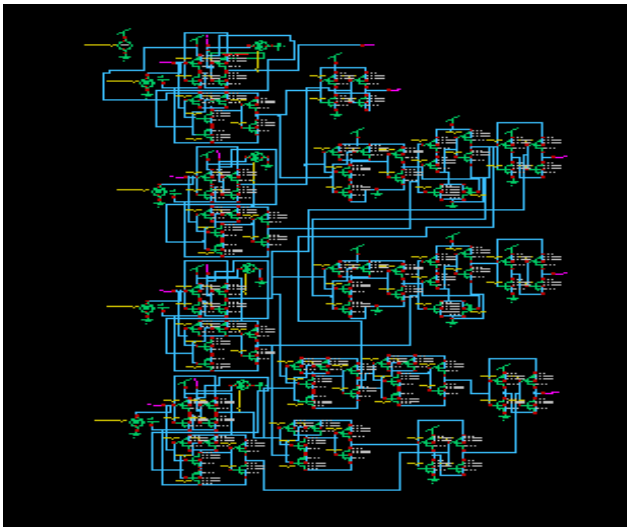

Figure 2: Schematic of Pipelined Han Carlson Adder

B.PIPELINED SPECULATOR

Two n-bit operands for addition are represented as A={A_0,A_1… A_N}, A={B_0,B_1… B_N} whereas, the sum, carry input and carry output are expressed as S=={S_0,S_1… S_N}, Cin and Cout respectively. Gate-level circuit diagram of the speculator used in adder design. This block is based on CLA logic to speculate the output carry for each 4-bit adder block.

Speculation is carried out for 'r' msb bits of each block where r is less than the size of block. Subsequently, the input carry for each speculator block is 0 or 1which introduces positive or negative errors respectively [6].The output carry, which is denoted as Cso, from each speculator block is fed as an input carry for the adder block succeeding it. Now, each 4-bit adder block need not wait for the input carry from the preceding 4- bit adder block as shown in figure3. Instead, all such adder blocks perform simultaneous additions on receiving input carries from the concerned speculator blocks. Speculator block computes carry based on the CLA equation.

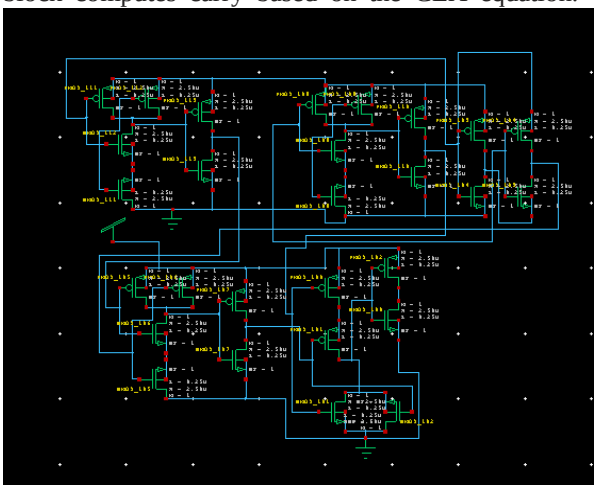

Figure 3: Schematic of Pipelined speculator

C.PIPELINED COMPENSATOR

The COMP block detects inconsistencies between speculated carry and expected carry from the previous sub adder with an XOR gate. This creates an error flag that triggers the activation of one of the two compensation techniques, namely error correction and error reduction found in [7]. The potential error always remains of the same nature as the input carry of the SPEC block as shown in figure4.

Thereafter, the output from XOR gate generates an error flag (f_e) that triggers the activation of one of the two compensation techniques, error correction and reduction. If the XOR-gate output is '0' then the local sum is directly passed to the final output found in [8]. Similarly, if the XOR gate gives '1' then this indicates that an error has occurred which can be either positive or negative.

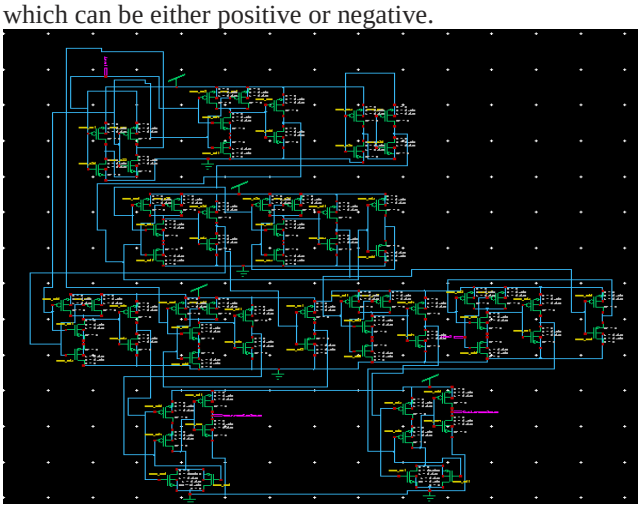

Figure 4: Schematic of Pipelined compensator

1)Incrementer Block: An incrementer is a circuit that is much simpler than an adder. A simple half adder that can be used to build an incrementer, which can be increment a single bit. The sum of two bits is computed by XOR, and if both bits are 1, there is a carry. Each carry-out is connected to the carry of the next-bit [8,9]. A 1 value is fed into the initial carry-in to start the increment. This increment can be done independent of a register by the means of a combinational circuit called binary incrementer.

2)Multiplexer Block: A multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has ⌈n⌉ select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. Multiplexers can also be used to implement Boolean functions of multiple variables.

3)Demultiplexer: A de-multiplexer is a device taking a single input signal and selecting one of manydata-output-lines, which is connected to the single input.

4)Clock gated: In sequential circuit one two-input AND gate is inserted in logic for clock gating. One input to AND gate is clock and while the second input is a signal used to control the output. The latch-free clock gating style uses a simple AND or OR gate. Here if enable signal goes inactive in between the clock pulse or if it multiple times then gated clock output either can terminate prematurely or generate multiple clock pulses found in [10]. This restriction makes the latch-free clock gating style inappropriate for our single-clock flip-flop based design.

IV. PERFORMANCE ANALYSIS OF PROPOSED ISA

Functional verification of proposed ISA is carried out on Tanner EDA tool as shown in figure7 and 8. It is a spice computer analysis programmed for analogue integrated circuits. Spice program provides facility to the use to design and simulate new ideas in analogue integrated circuits before going to the time consuming and costly process of chip fabrication.

Figure 5: Schematic of Conventional ISA

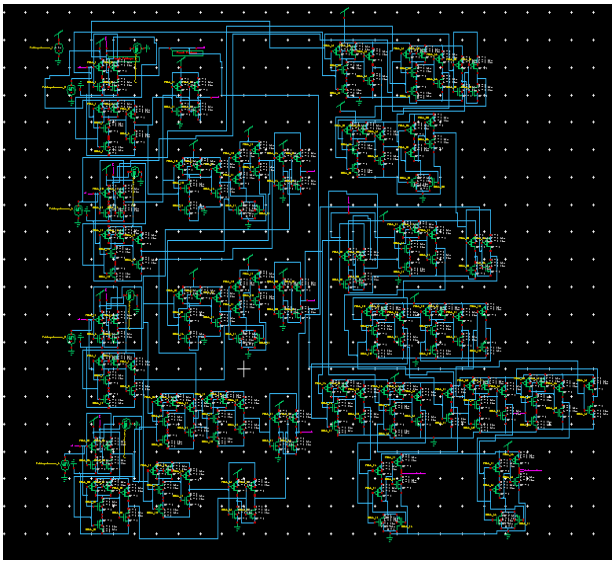

Figure 6: Schematic of Proposed ISA

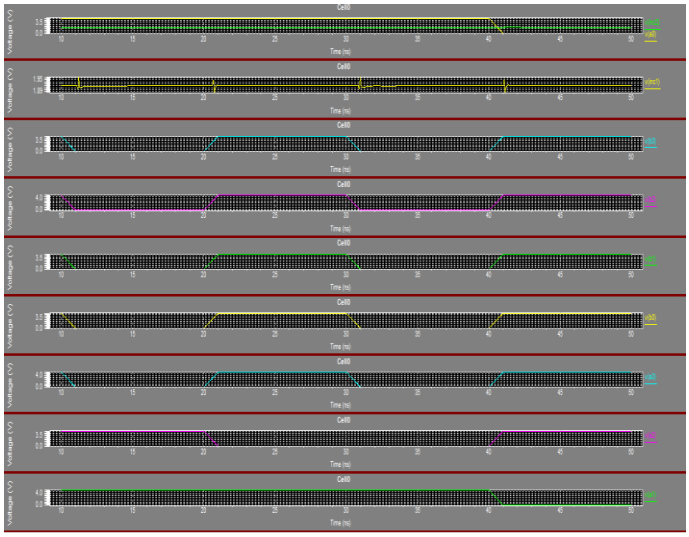

Figure 7: Proposed input of ISA

Table1:Performance Analysis

S.No	ISA STRUCTURE	POWER (mW)
1	Conventional Inexact Speculative Adder	16.01
2	Proposed Inexact Speculative Adder	14.22

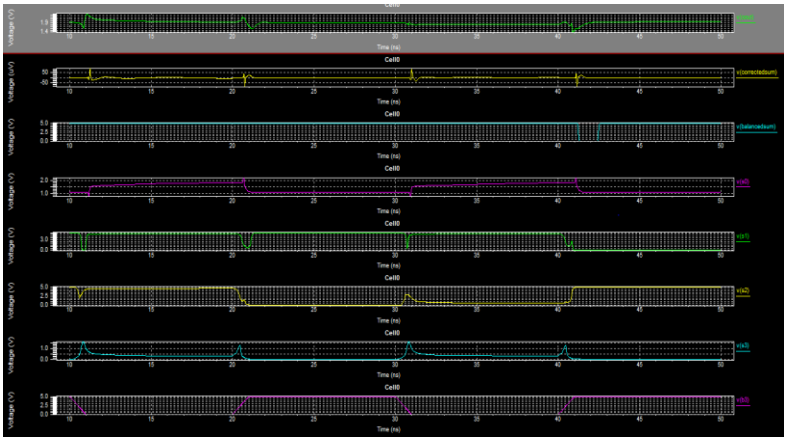

Figure 8: Proposed output of ISA

V. CONCLUSION

Thus the inexact speculative adder (ISA) has been designed based on Han Carlson adder (HCA) with high power and low speed. HCA is a fast parallel adder as it reduces the propagation delay and improves the speed as shown in Table 1. Also, this design is fine grain pipelined and clock gated to escalate speed and alleviate power consumption respectively. Simulation results showed that the proposed ISA can operate lower power compared with earlier reports.

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